AMENDMENT TO THE CLAIMS

Sub D1

1. (Currently amended) A semiconductor device comprising:

a first semiconductor region of a first conductivity type, defined by a first end surface, a second end surface opposing to the first end surface and ~~a~~ first and second side boundary ~~surface~~ surfaces connecting the first and second end surfaces;

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a second semiconductor region of the first conductivity type ~~connected~~ being in contact with said first semiconductor region at the second end surface;

a third semiconductor region of a second conductivity type ~~connected~~ being in contact with said first semiconductor region at the first end surface; and

a fourth semiconductor region having first and second inner ~~surface~~ surfaces in contact with the first and second side boundary ~~surface~~ surfaces respectively and an impurity concentration lower than said first semiconductor region, configured such that ~~the fourth semiconductor region surrounds said first semiconductor region,~~ the fourth semiconductor region is disposed between the second and third semiconductor regions.

2. (Original) The semiconductor device of Claim 1, wherein said fourth semiconductor region has the first conductivity type.

3. (Original) The semiconductor device of Claim 1, wherein outer surface of said fourth semiconductor region serves as a chip outer-surface of the semiconductor device and the chip outer-surface is substantially orthogonal with the second end surface of said first semiconductor region.

4. (Original) The semiconductor device of Claim 1, wherein said fourth semiconductor region is made of a wafer cut from bulk crystal.

5. (Currently amended) The semiconductor device of Claim 1, further comprising a first main electrode layer ~~is~~ formed on a bottom surface of said second semiconductor region.

6. (Currently amended) The semiconductor device of Claim 5, wherein said first main electrode layer is contacted with said second semiconductor region, ~~trough~~ through a first concavity formed at the bottom surface of said semiconductor region.

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7. (Original) The semiconductor device of Claim 1, further comprising a first main electrode layer, a part of the first main electrode layer ~~is~~ being buried in a via hole penetrating through said second semiconductor region, configured such that the buried part of the first main electrode layer contacts with said first semiconductor region.

8. (Currently amended) The semiconductor device of Claim 1, further comprising a second main electrode layer ~~is~~ formed on a top surface of said third semiconductor region.

9. (Currently amended) The semiconductor device of Claim 8, wherein said second main electrode layer is contacted with said third semiconductor region, ~~trough~~ through a second concavity formed at the top surface of said third semiconductor region.

10. (Withdrawn).

11. (Withdrawn).

12. (New) A semiconductor device comprising:

a first semiconductor region of a first conductivity type, defined by a first end surface, a second end surface opposing to the first end surface and first and second side boundary surfaces connecting the first and second end surfaces;

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a second semiconductor region of the first conductivity type having first and second upper surfaces;

a third semiconductor region of a second conductivity type being in contact with said first semiconductor region at the first end surface;

a fourth semiconductor region having first and second inner surfaces in contact with the first and second side boundary surfaces respectively and having first and second lower end surfaces in contact with said first and second upper surfaces respectively, and an impurity concentration lower than said first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions; and

a first main electrode layer, a part of the first main electrode layer being buried through said second semiconductor region, configured such that the buried part of the first main electrode layer contacts with said second end surface of said first semiconductor region.

Add D1 (claim 13)